H-754-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Accompanying Continuation Application under 37 CFR 1.53:

Prior Application: H. MURAYAMA et al
Serial No. 09/227,740
Filed: January 8, 1999

Group Art Unit: 2186
Examiner: T. Thai
For: INFORMATION PROCESSING APPARATUS

PRELIMINARY AMENDMENT

Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above application as follows.

IN THE SPECIFICATION

Page 1, before the first line, add the paragraph:

--This is a continuation application of U.S. Serial No. 09/227,740, filed January 8, 1999.--

IN THE CLAIMS

Cancel claim 1 without prejudice or disclaimer, and add new claims 21-40 as follows.

--21. A computer system, in which a part of main memory is able to be hot-plugged, said computer system comprising,

a first memory,

a non-volatile storage storing first memory information of said first memory size and a second memory information of a second memory to be hot-plugged,

a processor acquiring said first and second memory information from said non-volatile storage and mapping said first memory based on said first and second memory information.

--22. A computer system according to claim 21,

wherein said processor generating first logical-physical address translating table for said first memory based on said first and second memory information and stores at least a part of said first logical-physical address translating table in said first memory, and

wherein said processor assigns a region to store a second logical-physical address translating table for said second memory in said first memory.

--23. A computer system according to claim 22,

wherein said first memory has a non-translatable region, and

wherein said processor uses said non-translatable region for said first and second logical-physical address translating table.

--24. A computer system according to claim 22,

wherein said processor has TLB.

--25. A computer system according to claim 21,

wherein said non-volatile storage is EEPROM.

--26. A computer system comprising,

a first main memory,

a non-volatile storage storing a first configuration information of said first main memory and second configuration information of a second main memory to be hot-added, and

a processor acquiring said first and second configuration information form said non-volatile storage on memory-mapping of said first main memory.

--27. A computer system according to claim 26,

wherein said processor assigns non-address translated region in said first main memory on memory-mapping of said first main memory.

--28. A computer system according to claim 27,

wherein said processor determines size of said non-address translated region based on said first and second configuration information.

--29. A computer system according to claim 28,

wherein said processor generates a first logical-physical address translation pairs of said first main memory based on said first configuration information and stores at least a part of said logical-physical address translation pairs in said non-address translated region.

--30. A computer system according to claim 28,

wherein said processor assigns a region a second logical-physical address translating pairs of said main memory in said non-address translated region.

--31. A computer system according to claim 26,

wherein said non-volatile storage is EEPROM.

--32. A computer system according to claim 26,

wherein said processor has TLB.

--33. A computer system, which supports a virtual memory system, said computer system comprising,

a first main memory,

a non-volatile storage storing a first information setting a memory size of a second main memory to be hot-inserted,

a processor mapping said first main memory and acquiring said first information upon said mapping.

--34. A computer system according to claim 33,

wherein said processor assigns a top priority region of interrupt handling in said first main memory.

--35. A computer system according to claim 34,

wherein said processor acquires a memory size of said first main memory and determines said not priority region from said memory size of said first main memory and said first information.

--36. A computer system according to claim 35,

wherein said processor generates a first logical-physical address translation pairs of said first main memory and stores at least a part of said first logical-physical address translating pairs in said top priority region.

--37. A computer system according to claim 35,

wherein said processor reserves a region to store a second logical-physical address translation pairs of said second main memory in said top priority region.

--38. A computer system according to claim 33,

wherein said non-volatile storage EEPROM.

--39. A computer system according to claim 35,

wherein said processor has a logical-physical address translating unit.

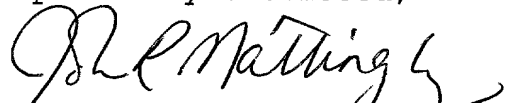
--40. A computer system according to claim 39,

wherein said processor has TLB.--

REMARKS

The Applicants request entry of the foregoing amendment.

Respectfully submitted,



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